An accurate large-signal model for a high-efficient Si bipolar GSM power transistor

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***Abstract* — We present an accurate large-signal modelling approach for Si bipolar RF power transistors. An equivalent circuit model of a state of the art GSM power transistor (900MHz, 3.5V, 4W, 70%) is constructed. The model is verified with accurate load pull measurements. Large-signal parameters (P_{out}, G_T, PAE) are predicted accurately.**

I. Introduction

Because of the world-wide increase of mobile communications, the market of power amplifiers (PA) for cellular phones (GSM, DCS1800, CDMA) has increased rapidly the past few years. The severe competition in this field drive a strong innovation rate (each new generation must be more cost effective, smaller, and have better performance) and short time-to-market, which necessitates the use of predictive design tools. As the performance of a PA is greatly set by the end stage transistor, it is very important to have a good electrical model of this transistor, that describes the large-signal parameters such as power gain and power added efficiency (PAE) correctly. In reference [1] simulations of a low-voltage 500mW silicon device at 1.8 GHz are compared with measurements. However, experimental verification for larger devices become much more difficult because of the very low impedances at both the in- and output that accompanies these large devices.

This paper describes an accurate large-signal modelling approach for silicon bipolar power transistors. The approach is illustrated and verified with accurate load pull measurements for a 3.5V, 4W power transistor operating at 900 MHz (GSM), as is used in state of the art PA modules.

II. Description of the RF power transistor

The power transistor described in this paper is made in a double poly-silicon bipolar technology with cut-off frequency of 25 GHz, and a collector-emitter breakdown of 5V [2]. The back-end consists of two metal layers. Fig. 1 shows a drawing of the power transistor. It is composed of 102 elementary npn cells in parallel, distributed in 6 large sections. Each elementary cell has two emitter fingers (30 μm long, and 0.4 μm wide), three base contacts, and two collector contacts. The total emitter length is 6120 μm. The total emitter ballast resistor is 54 mΩ. The parasitic collector-substrate junction capacitance is minimised by merging the buried layer (collector) of 17

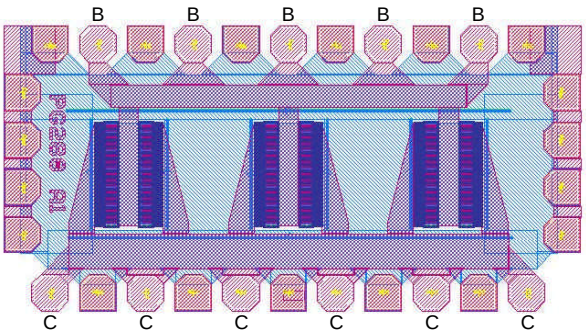

Fig. 1. Layout of the power transistor (operating at 4W, 900 MHz). The base and collector bondpads are indicated. The other bondpads are connected to the emitter. Size of the die: about 800x1500 μm.

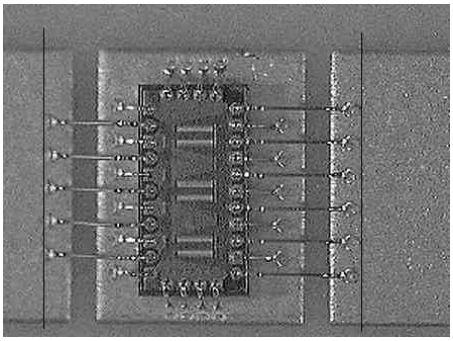

Fig. 2. Photograph of the power transistor mounted on a ceramic substrate and wire bonded. The black lines show the positions of the reference planes of the base (left) and collector (right) terminals.

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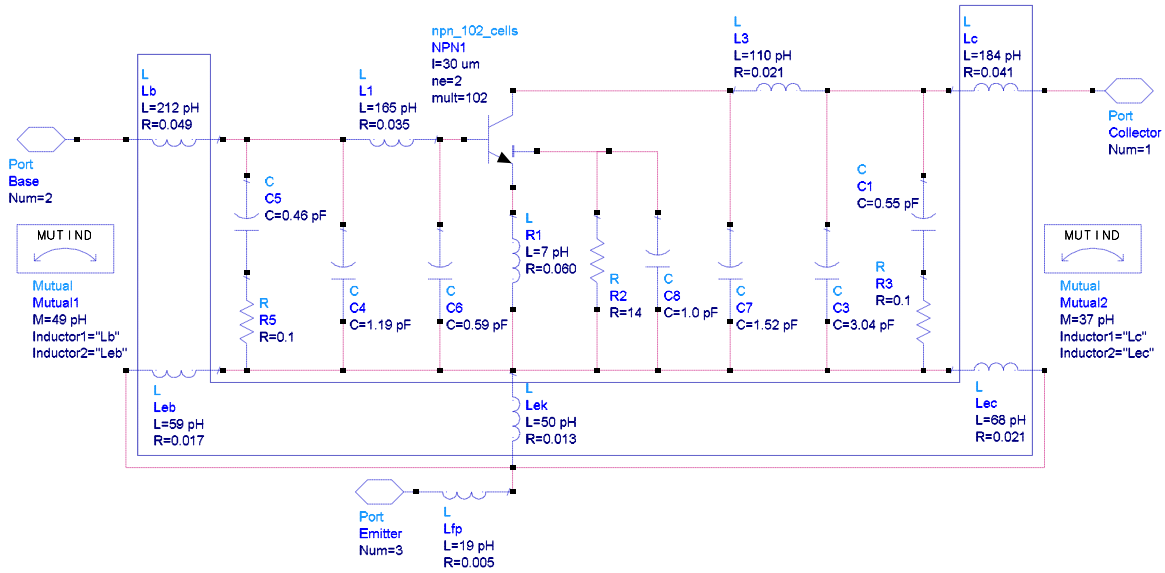

Fig. 3. Equivalent circuit of the electrical model used in the circuit simulator. The area inclosed by the dashed line indicate the lumped inductors used to represent the bondwires.

neighbouring cells. Along the edge of the die there are bondpads for the base (5x), collector (6x) and emitter (19x).

For evaluation the die is glued on a ceramic substrate with plated bonded copper metallization (Fig.2). Bondwires are used to connect the base, collector and emitter. The emitter is contacted to the back-side metallization of the substrate using six vias.

III. Modelling Approach

The goal is to define a large signal model of the power transistor as shown in Fig. 2 with reference planes as indicated. The segmentation approach was used to construct this model [3]. There are four segments defined: the active area, on-chip parasitics, bondwires, and the footprint of the ceramic substrate. Each segment is considered in more detail.

A. Active Area

The compact model MEXTRAM [4],[5] is used to model the active area of the transistor, which actually consists of 102 elementary npn cells in parallel. MEXTRAM parameters are extracted on one cell. Subsequently we assume that the intrinsic npn scales with the number of cells. Parameter extraction of the complete power transistor would cause self-heating or even thermal run-away, preventing a proper parameter extraction.

B. On-Chip Parasitics

The interconnect metallization on the die introduces parasitic capacitances, inductances and resistances around the transistor. It is very essential to characterise these parasitics correctly, because they have a major effect on the frequency response of the device and thus on impedance levels and large-signal performance.

The parasitic base-emitter and collector-emitter overlap capacitances are determined by measuring the total zero bias capacitances at in- and output of the device and subtracting the junction capacitance values, which are known from the MEXTRAM parameter extraction. The found capacitance values can be confirmed from parasitic extraction directly performed on the die layout.

The total inductance (interconnect, bondwires and footprint) was measured by biasing the transistor in hard-saturation (i_b = 1.0 A and i_c = i_e = -0.5 A) and measuring the S-parameters. The contribution of the bondwires and footprint are subtracted from the total inductance and the remaining inductance was contributed to the interconnect. This approach was used because there are no accurate inductance extraction tools for on-chip interconnect available at present.

The interconnect resistances are estimated by considering the layout and the sheet resistances of the metal layers.

Parasitic effects also occur in the silicon substrate of the die, e.g. the collector-substrate junction which is parallel at the output. Due to the high resistivity of the substrate (20 Ωcm) this capacitance is very lossy. Despite efforts to reduce this substrate resistance (by proper design of emitter-substrate contacts) it still plays an important role in the large-signal performance [1],[2]. Hence, a substrate model is required. In this work the parasitic substrate effects are modelled through a parallel RC network (R2, C8 in Fig. 3). The values are optimised on cold-state S-parameter measurements.

C. Bondwires

In the model of the power transistor the bondwires are represented by lumped inductors as can be seen in Fig. 3. The values of these inductors and their mutual coupling are determined by using a predictive bondwire model [6]. This generic bondwire model calculates the electrical behaviour of a set of wires with an arbitrary shape (determined by photographs). Note that there is a significant mutual coupling between the base-emitter and collector-emitter wires.

D. Footprint of Ceramic Substrate

The footprint consists of the metal sheet on which the die is mounted plus the six vias to the bottom metallization (ground plane) of the ceramic substrate. Each via has a diameter of 200 μm. EM simulations, and S-parameter measurements show that the vias have a total inductance of about 19 pH.

Finally all segments are combined to form the full equivalent circuit model of the power transistor (Fig. 3).

IV. Large-Signal Verification

A. Set-up

The large-signal parameters of the power transistor are measured under realistic operating conditions and compared with simulations of the electrical model. We used a semi-automated passive load pull set-up with in- and output tuners operating in the frequency range of 0.4 - 4.0 GHz. The ceramic substrate with the die is mounted in an RF test fixture (Argumens) with 3.5 mm launchers.

Because of the very low device impedances (typically 1Ω), a two step impedance matching is required. In addition to the tuners, pre-matching structures are patterned on the ceramic substrate, directly at the in- and output of the transistor. The pre-matching can be either quarter-wave lines or tapers. A TRL (Thru - Reflect - Line) calibration procedure accurately determines the S-parameters of these transformers. This method ensures that the impedance at the fundamental frequency is reproducible and well known at the reference planes down to below 1Ω [7]–[9]. Despite the fact that with the load pull set-up the impedances at the 2nd and 3rd harmonic frequencies can not be set independently, they are known and taken into account in the simulations.

A scalar power calibration procedure in the load pull software ensures an absolute output power level accuracy of less than 0.1 dB.

The load pull set-up is arranged to perform measurements in pulsed mode. The RF source as well as the base bias voltage are pulsed with a period of 4.6 ms, and a pulse length of 575 μs.

B. Measurements

For GSM, the transducer gain (G_T) and power added efficiency (*PAE*) are the most important transistor parameters. In order to measure these parameters, first a source pull is performed to match the input and find the (approximate) input impedance. Secondly, load pull measurements are done to find the load termination at which optimum efficiency is achieved. Both source and load pull measurements are done at constant output power, either at 2W or 4W. Finally, at the optimal source and load terminations power sweeps are performed.

The device is biased in (inverse [10]) class AB: V_b = 0.67V and V_c = 3.5V.

C. Results

Table 1 shows that the simulated optimum source impedance of the device agrees very well with the measured impedance, in particular when tuned for 4W output power. Also the optimum load impedances found by load pull simulations coincide very well with the experimentally determined impedance states.

Table 1. Comparison of measured and simulated optimum terminations at in- and output, for 2 and 4W output power. Z_L is optimised for PAE.

P_{out} (W)	Z_S (Ω) Meas.	Z_S (Ω) Sim.	Z_L (Ω) Meas.	Z_L (Ω) Sim.
2	0.6-j0.7	0.4-j0.7	3.0+j1.3	3.1+j1.8
4	0.6-j0.9	0.6-j0.9	2.2-j0.3	2.5-j0.1

Fig. 4 and Fig. 5 show measured and simulated power sweeps at 900 MHz, tuned at 4W and 2W, respectively. The source and load terminations (both fundamental and harmonic) which are taken into account in the simulations are based on measured values. The fit at the 4W tuned case is very good. At 2W the agreement is less: both G_T and *PAE* are too optimistic. Note the high efficiency of more than 70%, which is comparable with GaAs and SiGe HBTs [11],[12]. In order to investigate the validity of the model over the complete GSM band (880-915 MHz) also power sweeps at 850 and 950 MHz are performed. As can be seen in Fig. 6 and Fig. 7 the model is quite accurate in the whole frequency band up to 4W.

D. Discussion

The accuracy of the model is very good for this type of power transistor, but possible improvements can be made by taking into account self-heating and distributed effects. However, there should always be a fair trade-off between advanced model improvements and computing power. Obviously, it appears that the scaling of the active area works very well, and a simple equivalent circuit satisfies. Besides, self-heating effects are not taken into account in this model because we expect that this will hardly change the performance of this device. Thermal simulations on

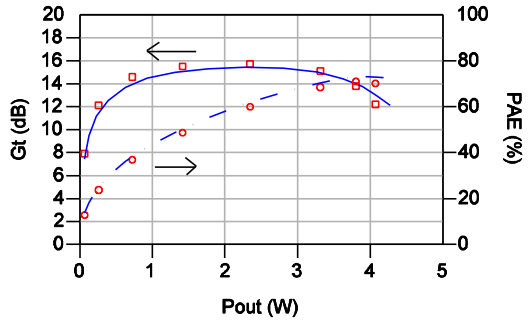

Fig. 5. Power sweep at 900 MHz, tuned at 4W.

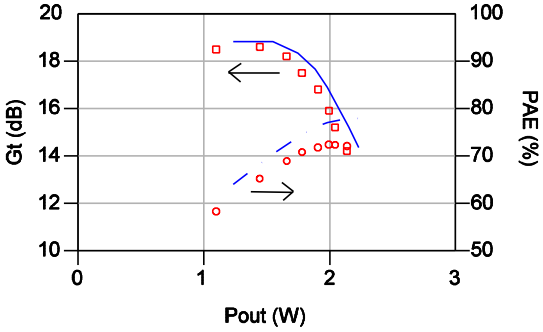

Fig. 5. Power sweep at 900 MHz, tuned at 2W.

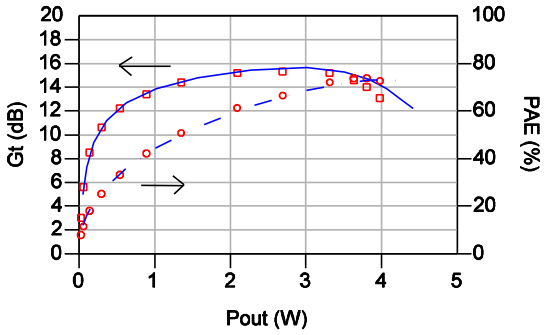

Fig. 7. Power sweep at 850 MHz, tuned at 4W.

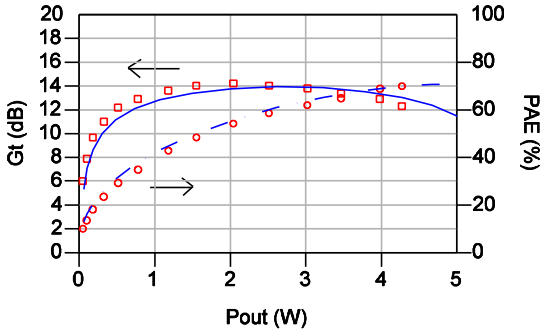

Fig. 7. Power sweep at 950 MHz, tuned at 4W.

the power die show that at 4W output power, 70% efficiency, and a duty cycle of 12.5% (1/8) the junction temperature reaches only 50°C at the end of the pulse [13].

Future investigations should make clear whether the modelling approach also works at higher frequencies (DCS1800) and higher duty cycles (3/8) or a more advanced approach is required.

V. Conclusion

For the first time we have shown the validity of an equivalent circuit model of a low-voltage silicon RF power transistor for GSM. Simulations are compared with accurate load pull measurements under realistic operating conditions and prove that the transducer gain and power added efficiency are described very well.

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